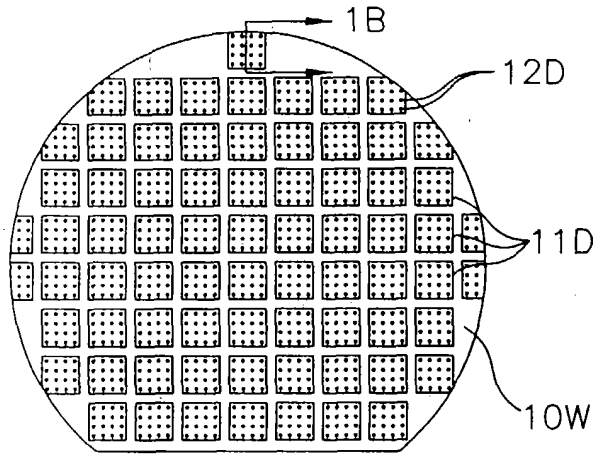

FIGURE 1A
(PRIOR ART)

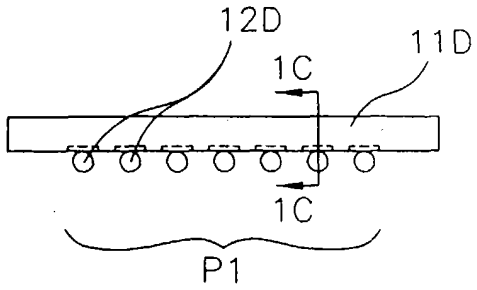

FIGURE 1B
(PRIOR ART)

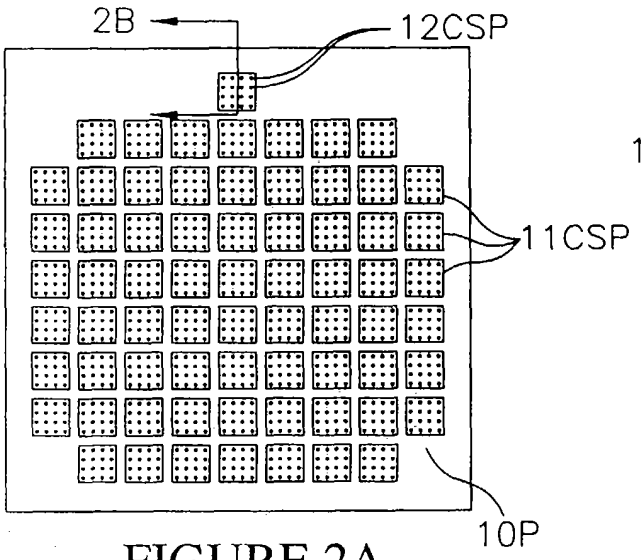

FIGURE 2A
(PRIOR ART)

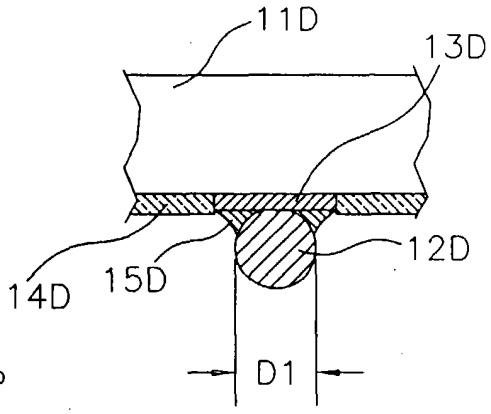

FIGURE 1C
(PRIOR ART)

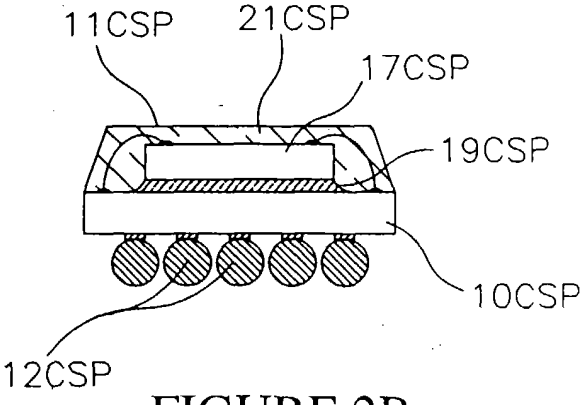

FIGURE 2B
(PRIOR ART)

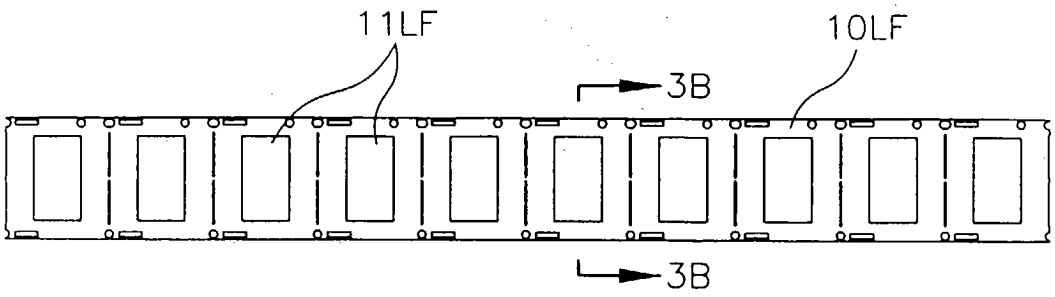

FIGURE 3A
(PRIOR ART)

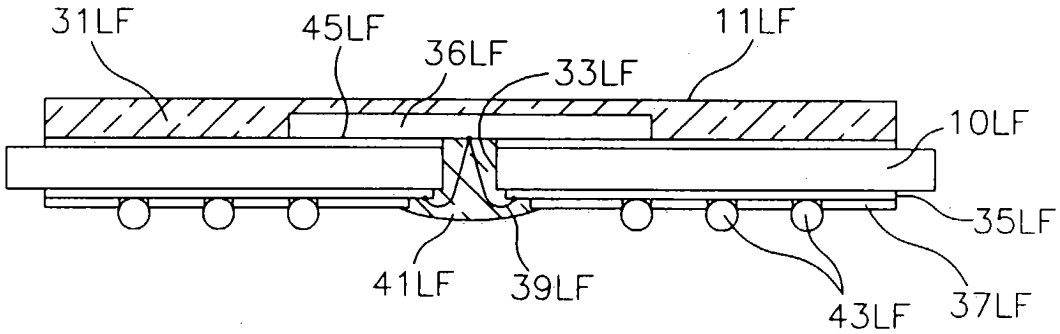

FIGURE 3B
(PRIOR ART)

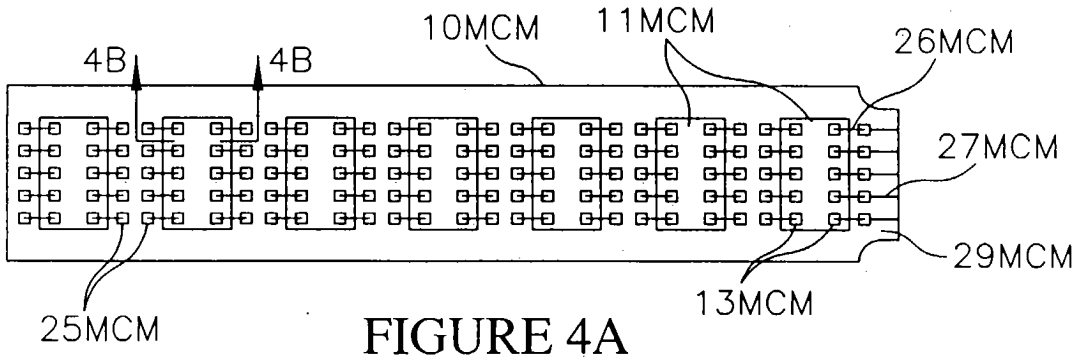

FIGURE 4A
(PRIOR ART)

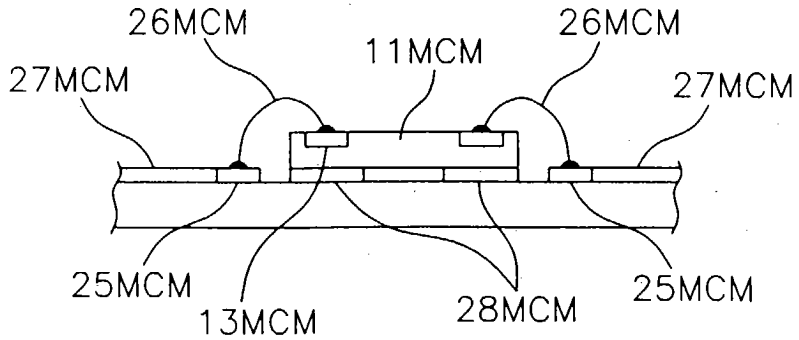

FIGURE 4B
(PRIOR ART)

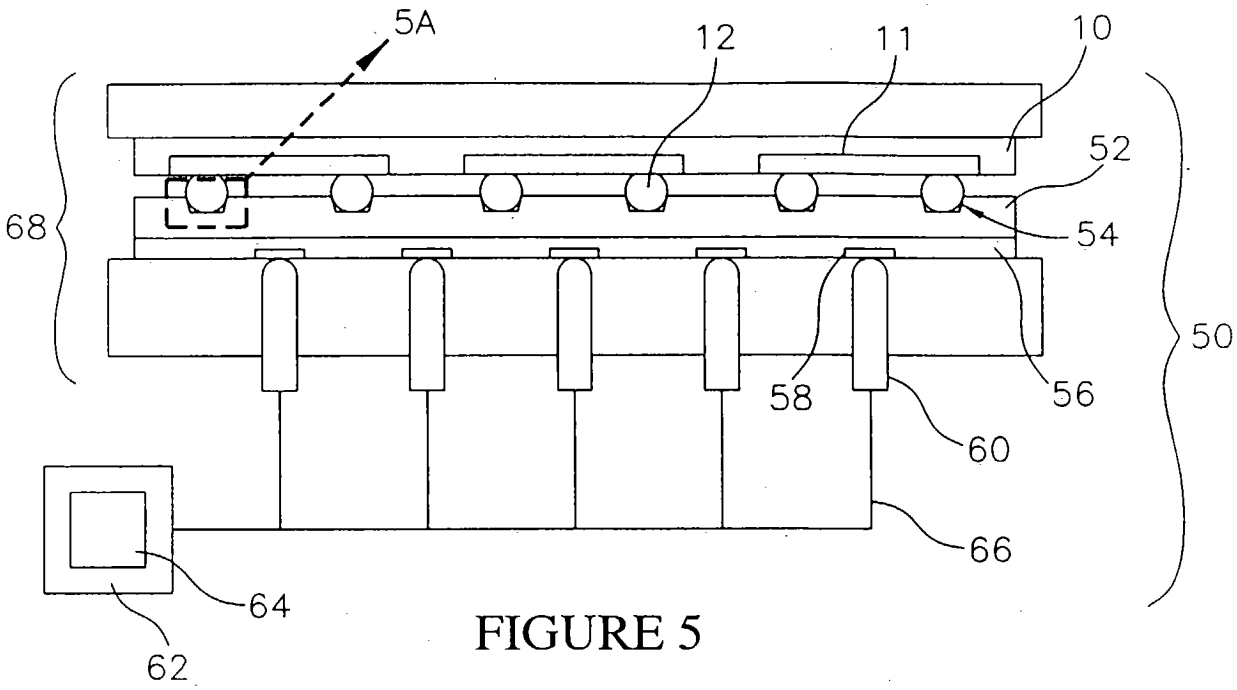

FIGURE 5

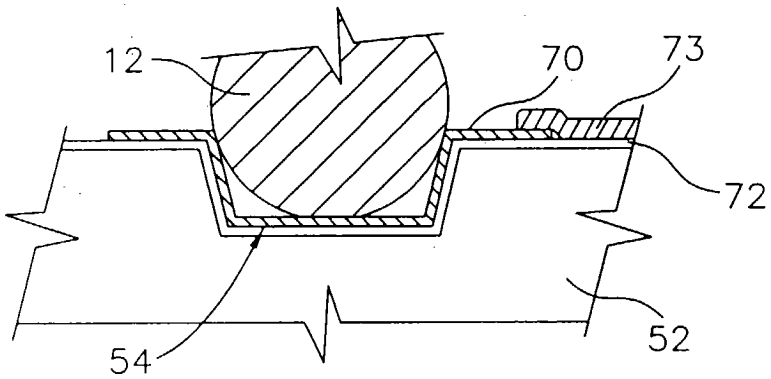

FIGURE 5A

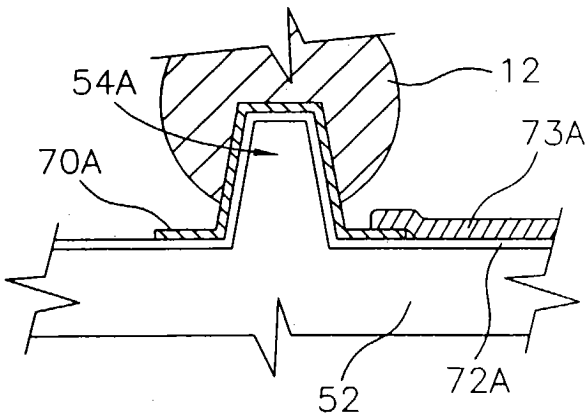

FIGURE 5B

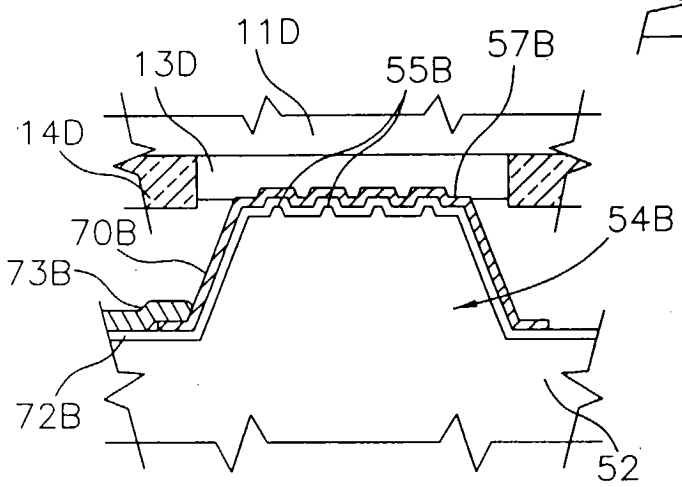

FIGURE 5C

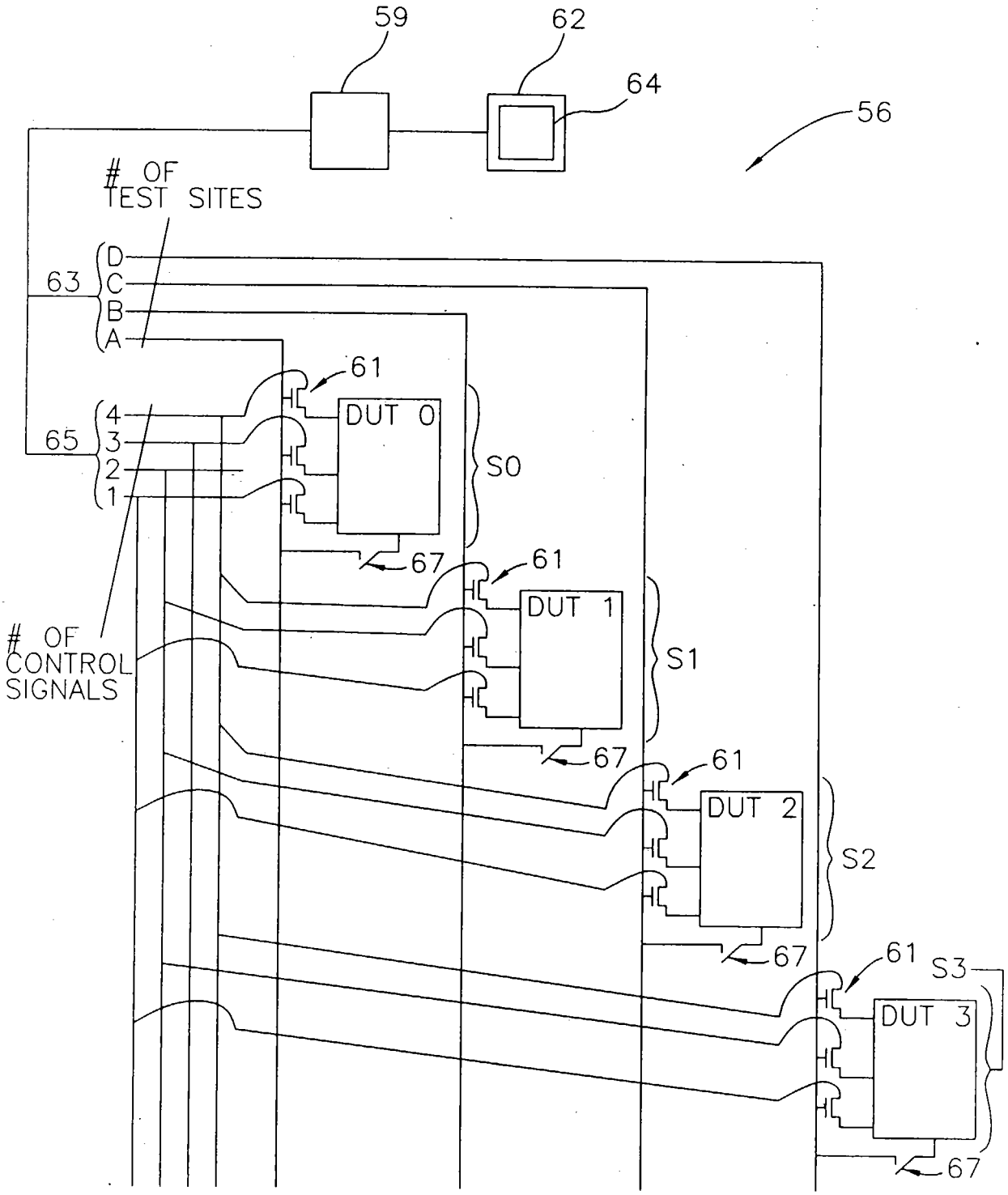
59
62
64
56
OF TEST SITES
63
D
C
B
A
61
DUT 0
65
4
3
2
1
S0
67
61
DUT 1
S1
OF CONTROL SIGNALS
67
61
DUT 2
S2
67
61
S3
DUT 3
67

FIGURE 6

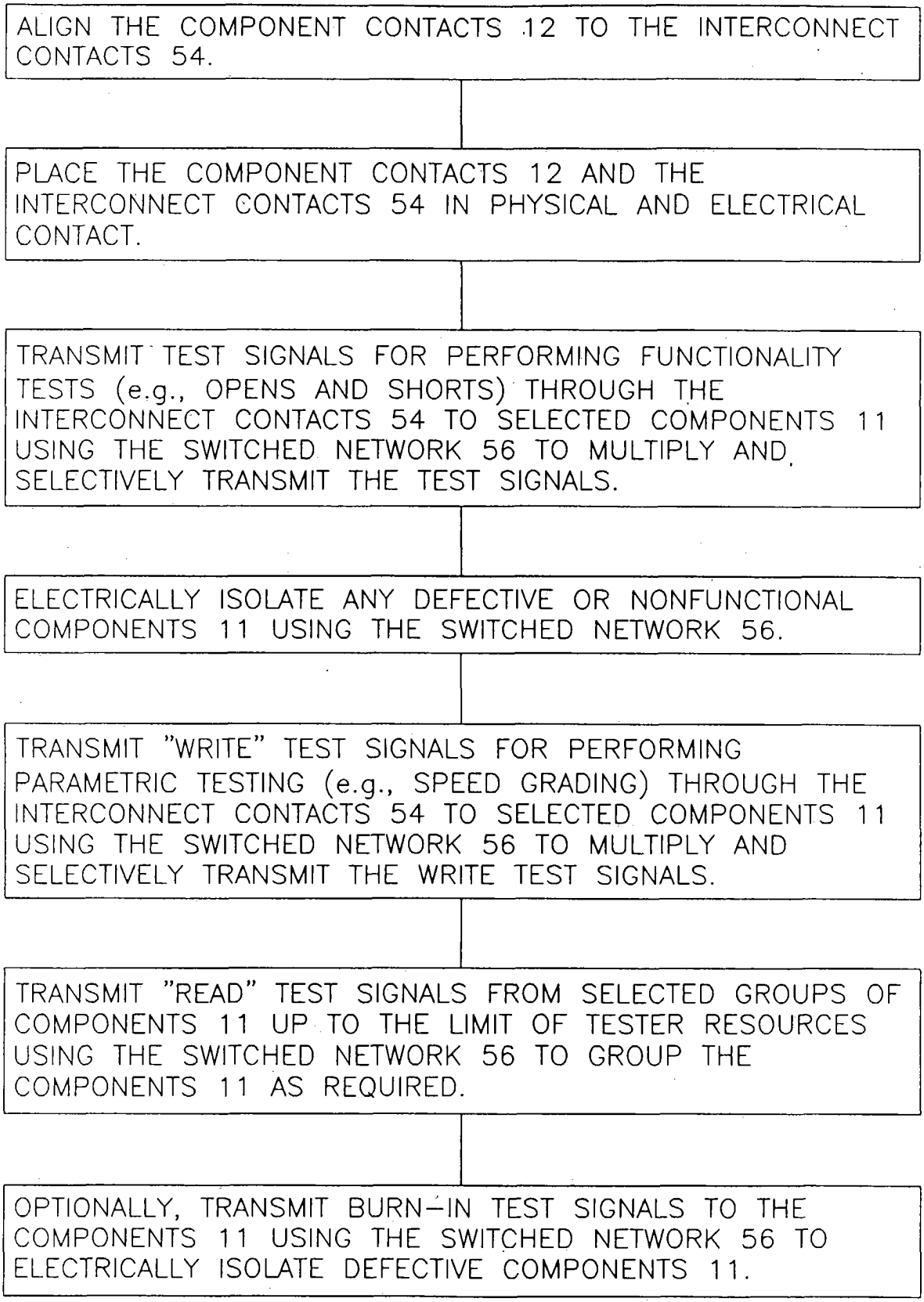
ALIGN THE COMPONENT CONTACTS 12 TO THE INTERCONNECT CONTACTS 54.
PLACE THE COMPONENT CONTACTS 12 AND THE INTERCONNECT CONTACTS 54 IN PHYSICAL AND ELECTRICAL CONTACT.
TRANSMIT TEST SIGNALS FOR PERFORMING FUNCTIONALITY TESTS (e.g., OPENS AND SHORTS) THROUGH THE INTERCONNECT CONTACTS 54 TO SELECTED COMPONENTS 11 USING THE SWITCHED NETWORK 56 TO MULTIPLY AND SELECTIVELY TRANSMIT THE TEST SIGNALS.
ELECTRICALLY ISOLATE ANY DEFECTIVE OR NONFUNCTIONAL COMPONENTS 11 USING THE SWITCHED NETWORK 56.
TRANSMIT "WRITE" TEST SIGNALS FOR PERFORMING PARAMETRIC TESTING (e.g., SPEED GRADING) THROUGH THE INTERCONNECT CONTACTS 54 TO SELECTED COMPONENTS 11 USING THE SWITCHED NETWORK 56 TO MULTIPLY AND SELECTIVELY TRANSMIT THE WRITE TEST SIGNALS.
TRANSMIT "READ" TEST SIGNALS FROM SELECTED GROUPS OF COMPONENTS 11 UP TO THE LIMIT OF TESTER RESOURCES USING THE SWITCHED NETWORK 56 TO GROUP THE COMPONENTS 11 AS REQUIRED.
OPTIONALLY, TRANSMIT BURN-IN TEST SIGNALS TO THE COMPONENTS 11 USING THE SWITCHED NETWORK 56 TO ELECTRICALLY ISOLATE DEFECTIVE COMPONENTS 11.

FIGURE 7

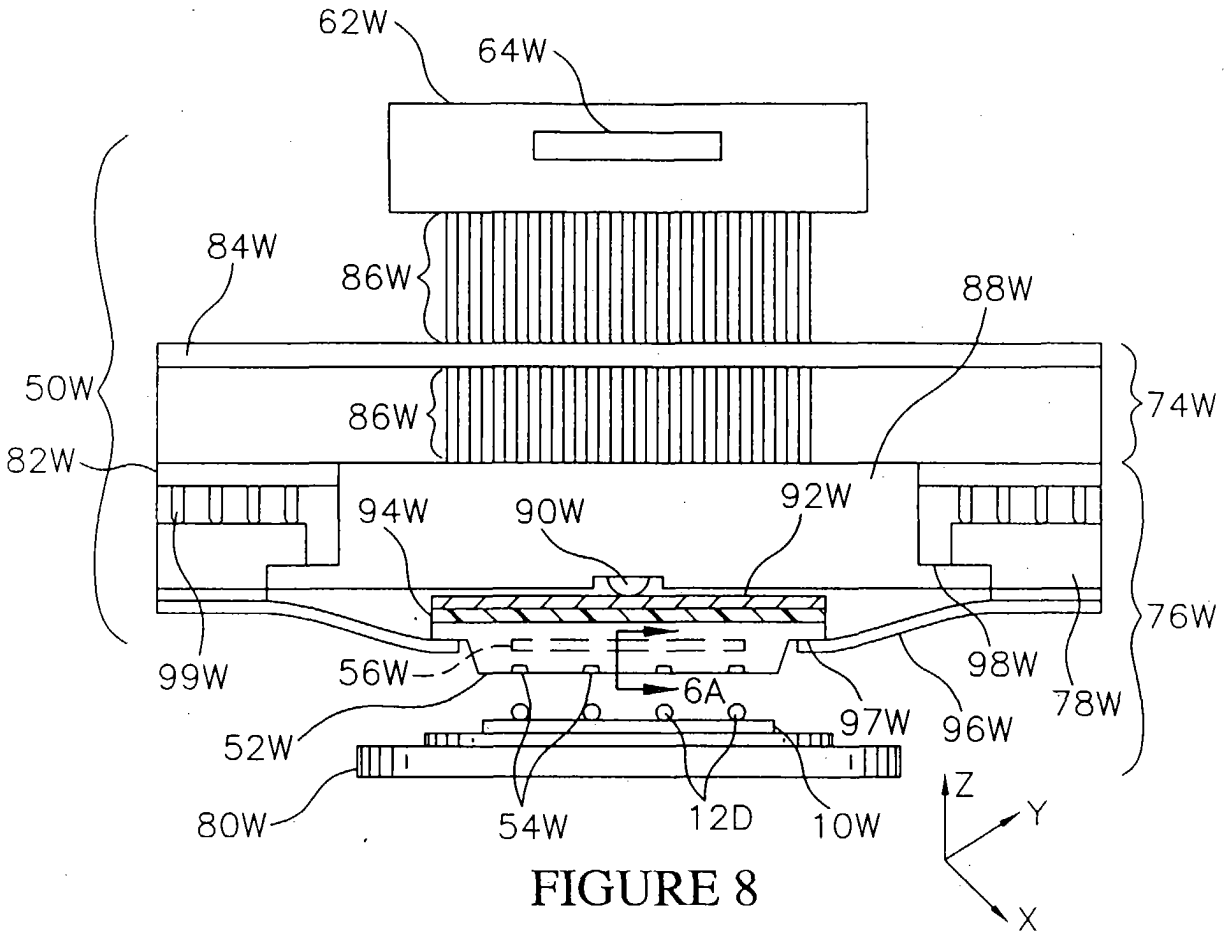

FIGURE 8

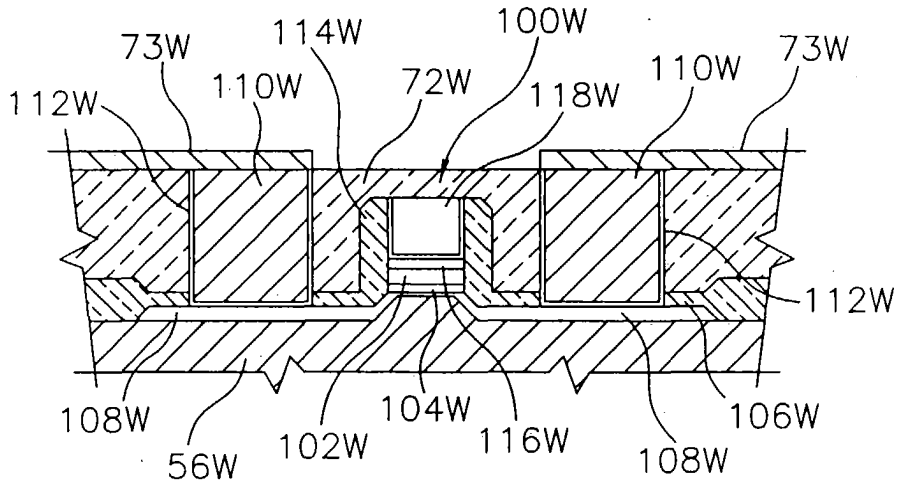

FIGURE 8A

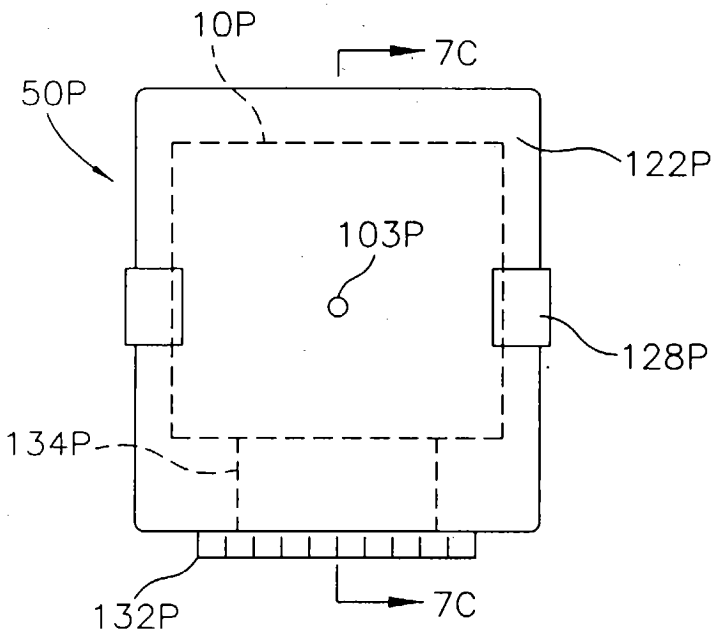

FIGURE 9A

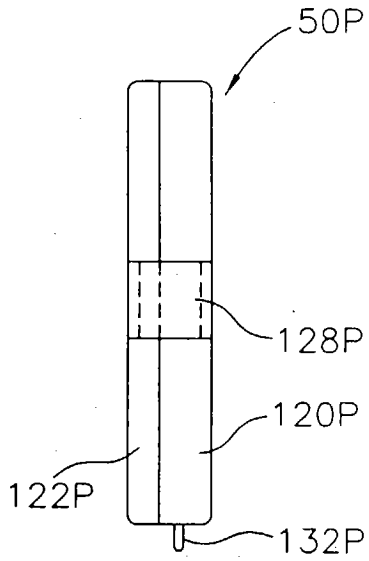

FIGURE 9B

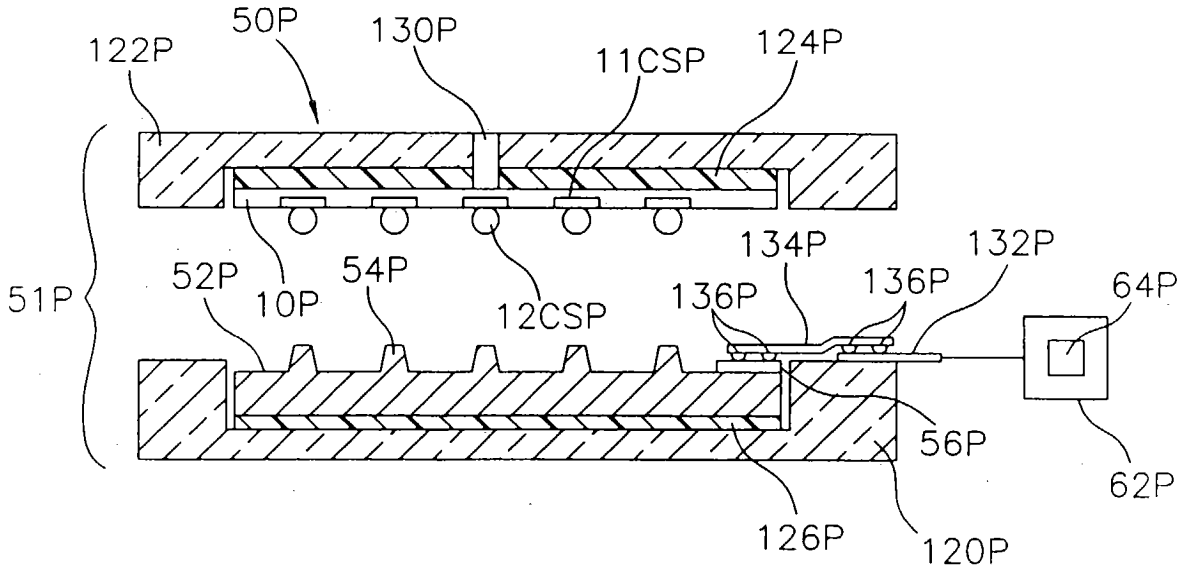

FIGURE 9C

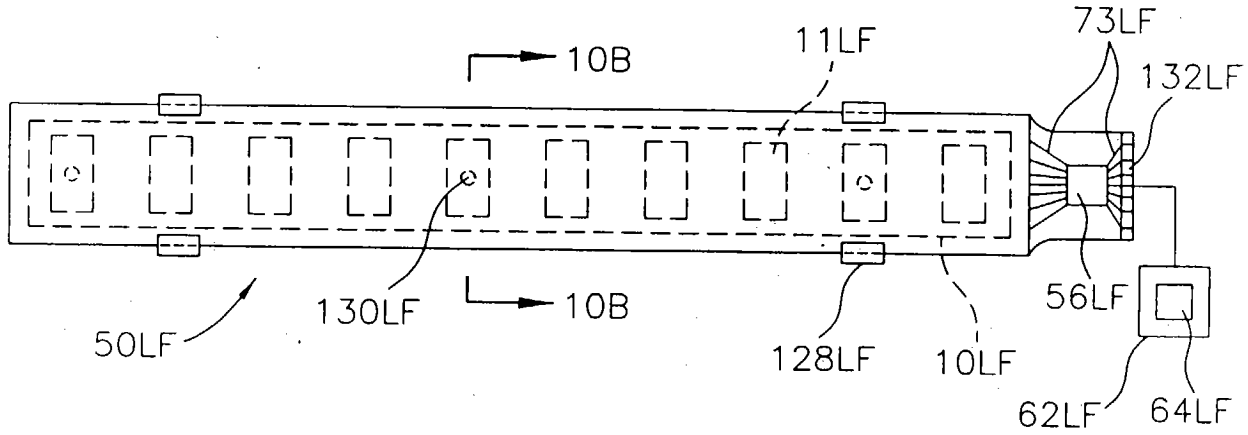

FIGURE 10A

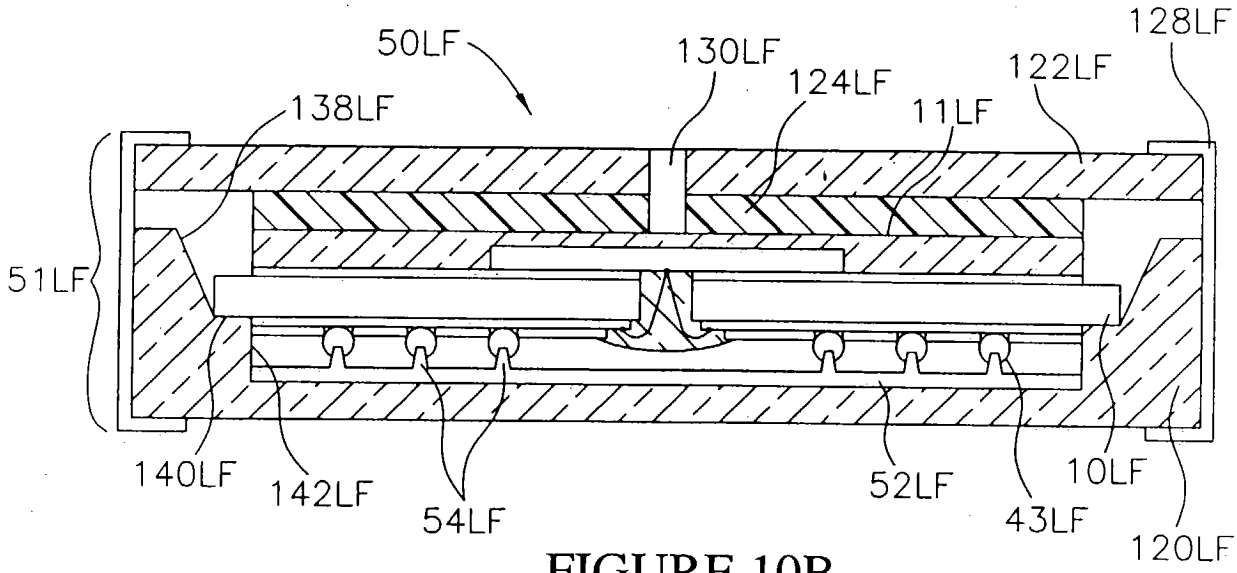

FIGURE 10B